

April 2004 Revised January 2005

### FSAV332

## Wide Bandwidth Video Switch

### **General Description**

The Fairchild video switch FSAV32 is a quad high speed video switch. Low On Resistance allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as four 1-bit switches with separate output enable (OE) pins. When OE is LOW, the switch is ON and Port A is connected to Port B. When OE is HIGH, the switch is OPEN and a HIGH-Impedance state exists between the two ports.

### **Features**

- Wide bandwidth: 368 MHz
- -84 dB non adjacent channel crosstalk at 10MHz
- -49 dB Off Isolation at 10MHz
- $3\Omega$  typical On Resistance (R<sub>ON</sub>)
- Low power consumption (3uA maximum)
- Control input: TTL compatible

### **Applications**

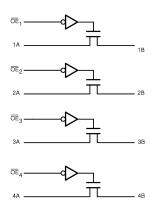
 Y/C video or CVBS video switch in LCD, plasma, and projector displays

### **Ordering Code:**

Order Number	Package Number	Package Description
FSAV332QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSAV332MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
FSAV332MTC_NL	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

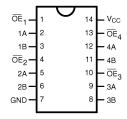
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. Pb-Free package per JEDEC J-STD-020B.

### **Logic Diagram**



## **Connection Diagrams**

### Pin Assignment for TSSOP



### Pin Assignment for QSOP



## **Pin Descriptions**

Pin Name	Description			
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3, \overline{OE}_4$	Bus Switch Enables			
1A, 2A, 3A, 4A	Bus A			
1B, 2B, 3B, 4B	Bus B			
NC	Not Connected			

## **Truth Table**

Inputs	Inputs/Outputs				
ŌĒ	A,B				
L	A = B				
Н	Z				

### **Absolute Maximum Ratings**(Note 1)

# Recommended Operating Conditions (Note 3)

Thermal Resistance (TSSOP) 12

(TSSOP) 115°C/W (TSSOP) 127°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float

### DC Electrical Characteristics All typical values are for V<sub>CC</sub> = 5V @ 25°C unless otherwise specified.

Symbol	Parameter	v <sub>cc</sub>	TA	=-40 °C to +8	5 °C	Units	Conditions
		(V)	Min	Тур	Max		
V <sub>ANALOG</sub>	Analog Signal Range	4.75 to 5.25	0		2.0	V	
V <sub>IK</sub>	Clamp Diode Voltage	4.75			-1.2	V	I <sub>IN</sub> = -18 mA
V <sub>IH</sub>	Input Voltage HIGH	4.75 to 5.25	2.0			V	
V <sub>IL</sub>	Input Voltage LOW	4.75 to 5.25			0.8	V	
I <sub>IN</sub>	Control Input Leakage	5.25			±1.0	μΑ	V <sub>IN</sub> = 0V to V <sub>CC</sub>
l <sub>OZ</sub>	OFF State Leakage Current	5.25			±1.0	μΑ	0 ≤ A, B ≤ V <sub>CC</sub>
R <sub>ON</sub>	Switch On Resistance	4.75		3.0	7.0	Ω	$V_{IN} = 1V, R_L = 75\Omega, I_{ON} = 13 \text{ mA}$
	(Note 4)	4.75		7.0	10.0	32	$V_{IN} = 2V, R_L = 75\Omega, I_{ON} = 26 \text{ mA}$
I <sub>CC</sub>	Quiescent Supply Current	5.25			3.0	μΑ	V <sub>IN</sub> = 0V V <sub>CC</sub> or I <sub>OUT</sub> = 0

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

## $\textbf{AC Electrical Characteristics} \text{ All typical value are for V}_{CC} = 5 \text{V} @ 25 ^{\circ}\text{C unless otherwise specified}.$

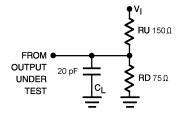
Symbol	Parameter	$V_{CC}$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			+85°C	Units	Conditions	Figure
		(V)	Min		Max	Ointo	Conditions	Number
t <sub>ON</sub>	Turn ON Time	4.75 to 5.25	1.0		5.0	ns	$V_I = 7V$ for $t_{PZL}$ and $V_I = OPEN$ for $t_{PZH}$	Figures 1, 2
t <sub>OFF</sub>	Turn OFF Time	4.75 to 5.25	1.0		5.0	ns	$V_I = 7V$ for $t_{PLZ}$ and $V_I = OPEN$ for $t_{PHZ}$	Figures 1, 2
t <sub>PLH</sub>	Propagation Delay	4.75 to 5.25			0.1	ns	V <sub>I</sub> = OPEN	Figures
$t_{PHL}$	(Note 5)	4.73 10 3.23			0.1	115	VI = OI EIV	1, 2
DG	Differential Gain	4.75 to 5.25		0.29		%	$R_L = 150\Omega$ , $f = 3.58MHz$	
DP	Differential Phase	4.75 to 5.25		0.10		Degree	$R_L = 150\Omega$ , $f = 3.58MHz$	
O <sub>IRR</sub>	OFF-Isolation	4.75 to 5.25		-84.0		dB	$f = 10MHz$ , $RL = 150\Omega$	Figure 3
X <sub>TALK</sub>	Non Adjacent Channel Crosstalk	4.75 to 5.25		-54.0		dB	$R_L = 150\Omega$ , $f = 10MHz$	Figure 4
BW	-3dB Bandwidth	4.75 to 5.25		368		MHz	$R_L = 150\Omega$	Figure 5

Note 5: This specification is guaranteed by design.

## Capacitance

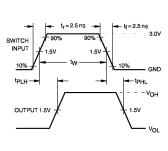
Symbol	Parameter	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		
		Тур	Units	Conditions
C <sub>IN</sub>	Control Pin Input Capacitance	3.0	pF	V <sub>CC</sub> = 5.0V
C <sub>ON</sub>	A/B ON Capacitance	30.0	pF	V <sub>CC</sub> = 5.0V, OE = 0V
C <sub>OFF</sub>	Port B OFF Capacitance	5.0	pF	V <sub>CC</sub> and OE = 5.0V

## **AC Loading and Waveforms**



Note: Input driven by 50  $\Omega$  source terminated in 50  $\Omega$  Note:  $C_L$  includes load and stray capacitance Note: Input PRR = 1.0 MHz,  $t_W$  = 500ns

FIGURE 1. AC Test Circuit



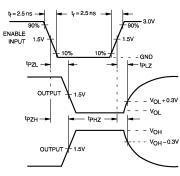


FIGURE 2. AC Waveforms

## **Test Diagrams**

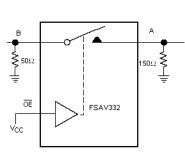


FIGURE 3. OFF Isolation Test

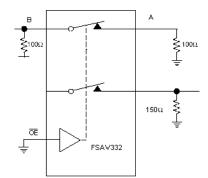


FIGURE 4. Crosstalk Test

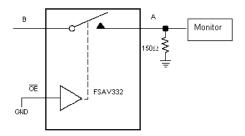
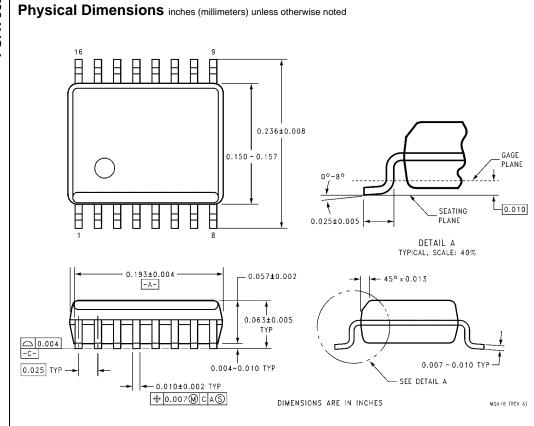
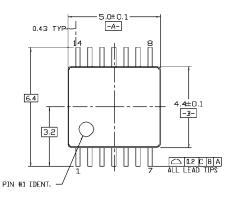


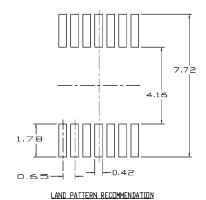
FIGURE 5. Bandwidth Test

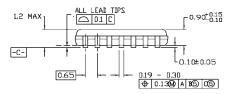


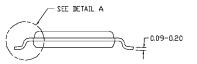
16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide Package Number MQA16

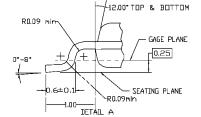
## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)











#### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ABREF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
- AND TILE BAR EXTRUSIONS

  D. DIMENSIONING AND TOLERANCES PER ANSI
  Y14.5M, 1982

MTC14revD

# 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

### **Technology Description**

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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